STi5289

QPSK demodulator and advanced SD decoder SoC for set-top boxes

Data brief

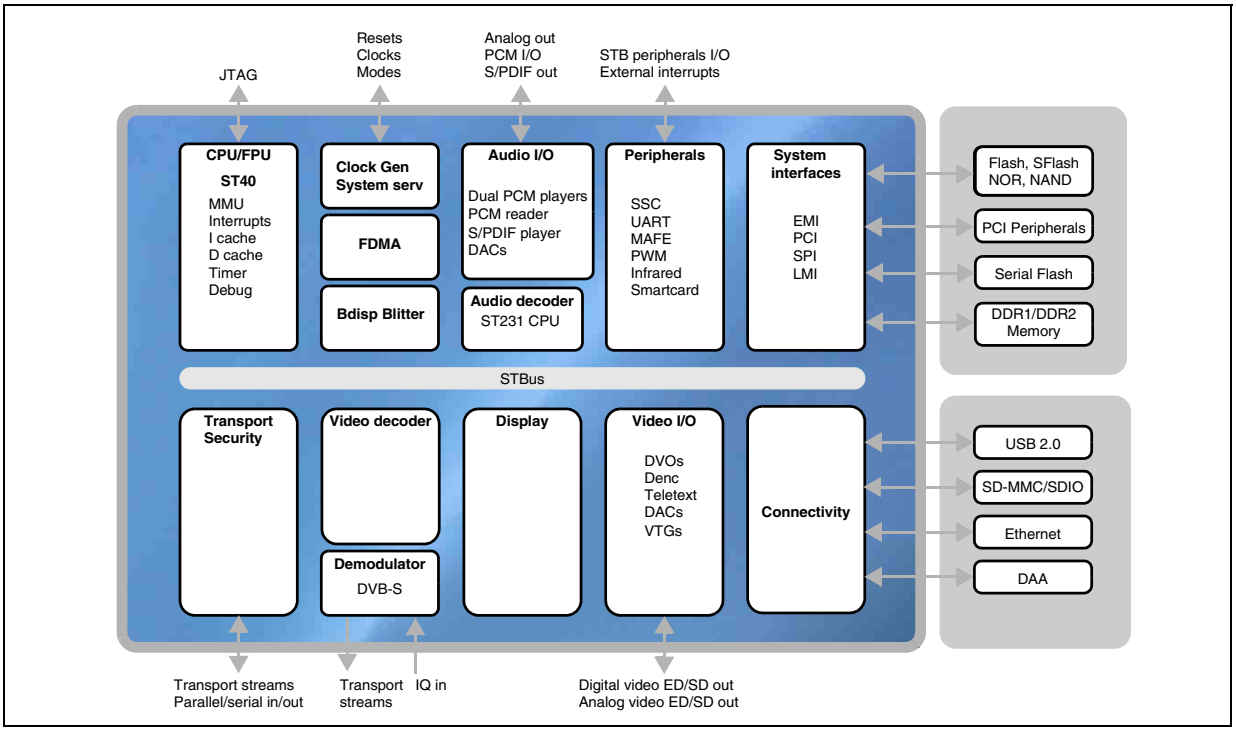
Features

- QPSK demodulation and DiSEqC™ 2.0 controller
- Advanced standard-definition video decoding (H264/VC-1/MPEG2/AVS)
- Advanced multi-channel audio decoding (MPEG 1, MPEG 2, MP3, DD/DD+, AAC/AAC+, WMA9/WMA9Pro)
- Linux, Windows CE® and OS21 compatible ST40 applications CPU
- 16-bit DDR1/DDR2 compatible local memory interface
- Multi-stream, DVR capable transport stream processing
- Extensive connectivity (dual USB controller, Ethernet MAC/MII/RMII/TMII, PCI and SD-MMC/SDIO)

Description

The STi5289 uses ST's state-of-the-art process technology to provide a low-cost, fully featured advanced decoding SD set-top box SoC.

It is a highly integrated solution suitable for DVB-S satellite/x-DSL/IP STB markets worldwide.



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1 Introduction

The STi5289 is targeted at the latest operator and CE manufacturer requirements for satellite STBs that use advanced decoding (H264/VC-1/MPEG2), and which conform to DVB, CEA and ITU specifications.

The STi5289 provides a solution for operators to specify a range of low-cost SD STBs including low-cost zappers, interactive STBs and DVR-capable STBs, with content delivery possible using satellite broadcast or broadband networks, or both (Hybrid STBs).

The STi5289 is optimized for secure Pay-TV applications with integrated DVB, DES, AES, Multi-2 and ICAM descramblers and smartcard interfaces.

The STi5289 offers enhancements in performance, features and integration to current users of ST's SD AVC family of audio/video decoders, while reducing cost and time-to-market for the next generation deployments.

Features	Benefits
Combines a DVB-S demodulator with STB decoding and display functions	This highly integrated SoC helps to reduce board area and manufacturing cost, allowing low-cost and small-size STBs to be designed for DVB-S networks
Serial Flash based secure boot and code storage, integrated voltage regulator, 23 mm x 23 mm PBGA package	Enables further BOM optimization and cost reduction of advanced decoding SD STBs
ST40 applications CPU, 32K I cache, 32K D cache	Superscalar performance from a single CPU core, using standard tools and operating systems (Linux, OS21)
STMicroelectronics' video decoding system with ST231 processor	Decoding of advanced standard definition MPEG2, H264 and VC-1/WMV9 streams, with the performance and flexibility for web-based content decoding such as Flash, DivX, MJPEG and Real
Dual USB 2.0 hosts, Ethernet MAC with MII/RMII and TMII, PCI, SD-MMC/SDIO	Extensive high speed connectivity for the widest range of STB peripherals, such as Flash drives, external HDDs, home network controllers (for example MoCA, Wi-Fi), memory cards
Low-power process, design and architecture	Best-in-class, low-power standby mode, to meet emerging energy standards for STBs. Dynamic configuration of power to individual sub-systems enables power-efficient active standby modes
Advanced 2D graphics and display subsystem and 480p/576p display output	Allows visually appealing user interfaces and video rich navigation to be offered to consumers, while high quality progressive output can be watched on the latest displays

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
30-Sep-2009	1	Initial release.
09-Oct-2009	2	Updates.
10-Jan-2011	3	Content reduced and simplified.

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